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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,862	03/31/2004	Jerrell P. Hein	75622P000102	5623

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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2646	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,862	HEIN ET AL.	
	Examiner	Art Unit	
	Walter F. Briney III	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7,10,11,13-16 and 18* is/are rejected.

7)☒ Claim(s) *2,6,8,9,12,17,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/18/2005
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1, 4, 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhou (US Patent 6,219,417).**

Claim 1 is limited to *an integrated circuit package apparatus*. Zhou discloses a direct current feed system as seen in figure 3. See Abstract. The disclosure of Zhou is directed primarily toward decreasing the fabrication size of a telephone line card. To this end, Zhou replaces all analog battery control circuitry that is normally associated with each respective SLIC (see figure 2) with a single digital signal processor that is shared with a plurality of SLIC devices located on a single line card (figure 3). Figures 5A and 5B depict in greater detail the system of figure 3, and clearly illustrate that each line card comprises a plurality of integrated circuits. In particular, a quad converter (e.g. 506[1]) interfaces four XASLIC devices (504[1]-504[4]) to a single DSP (508). The quad converter corresponds to the *integrated circuit*. Each XASLIC includes at least seven different connections between the quad converter. As disclosed by Zhou, one is for a *sensed tip signal* I_A, and a second is for a *sensed ring signal* I_B. See column 5, line 55, through column 6, line 10; and column 6, line 59, through column 7, line 1. Upon

receiving said signals, the quad converter passes them to the DSP. The DSP detects ring trip status using the I_A and I_B signals, and subsequently a *control signal* used for DC feed control that is converted to *analog* and *generated* at the output of the quad converter and fed to each XASLIC. See column 10, line 60, through column 12, line 32; figure 7, step 718; and all of figure 9. Clearly, each block is a discrete integrated circuit. Therefore, Zhou anticipates all limitations of the claim.

Claim 4 recites essentially the same subject matter as claim 1. The *sense circuitry* used for generating the tip and ring currents I_A and I_B includes the external loop feed resistors. See column 5, lines 55-61. The *power circuitry* is disclosed as residing within each XASLIC. See column 5, lines 61-64. Therefore, Zhou anticipates all limitations of the claim.

Claim 13 recites essentially the same subject matter as claim 1, and is rejected for the same reasons.

Claim 15 recites essentially the same subject matter as claim 4, and is rejected for the same reasons.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou (US Patent 6,219,417) in view of AM79213/Am79C203/031 Advanced Subscriber Line Interface Circuit (ASLIC™) Device Advanced Subscriber Line Audio-Processing Circuit (ASLAC™) Device Preliminary Datasheet," Publication #19770, Rev. B, September 1998, page 13.**

Claim 3 is limited to *the apparatus of claim 1*, as covered by Zhou. Zhou simply does not disclose the logic family used to manufacture the circuitry depicted in figures 5A and 5B. Therefore, Zhou anticipates all limitations of the claim with the exception *wherein the integrated circuit is a complementary metal oxide semiconductor (CMOS) integrated circuit.*

The examiner takes Official Notice of the fact that CMOS technology was well known at the time of the invention and was readily applied to both digital and analog circuits to provide low power and reliable integrated circuits. The AMD Preliminary Datasheet provides evidence that it was known to create CODECs using CMOS processes at the time of the invention.

It would have been obvious to one of ordinary skill in the art to fabricate the integrated circuits of figures 5A and 5B using CMOS technology as was known in the art for the purpose of implementing a low power and reliable telephone line card.

Claim 14 recites essentially the same subject matter as claim 3, and is rejected for the same reasons.

3. **Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou (US Patent 6,219,417) in view of Cotreay (US Patent 5,528,682).**

Claim 5 is limited to *the subscriber loop linefeed driver of claim 4*, as covered by Zhou. Made clear by the figures is the absence of any disclosure pertaining to the exact structure of the current sensing circuitry used to generate signals I_A and I_B besides the suggestion that a voltage differential is taken across the line feed resistors. Therefore, Zhou anticipates all limitations of the claim with the exception of *a pair of tip sampling resistors* and *a pair of ring sampling resistors.*

In accordance with the disclosed current detecting details of Zhou, Cotreay provides a prior art means of converting two differential voltages into a signal corresponding to a single line current. As seen in figure 4 of Bijman, a differential voltage sampled from two ends of a feed resistor (40) is fed into *a pair of sampling resistors* (66) and (68) and converted into a current signal at the output of an operational amplifier (36). In this manner, generation of currents I_A and I_B can be realized with circuitry that is isolated from the tip and ring lines, mitigating interference to the normal operation of the lines line card.

It would have been obvious to one of ordinary skill in the art to generate a signal representing a line current from a differential voltage measurement using the current detector presented in figure 4 of Cotreay simply because Zhou does not specifically disclose how to do so while requiring such an effect and because the sampling resistors (66) and (68) isolate the current detector from the tip and ring lines.

Claim 16 recites essentially the same subject matter as claim 5, and is rejected for the same reasons.

4. Claims 7, 10, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou (US Patent 6,219,417) in view of Rosch et al. (US Patent 5,274,702).

Claim 7 is limited to *the subscriber loop linefeed driver of claim 4*, as covered by Zhou. Again, Zhou discloses the existence of DC feed circuitry, but does not detail the structure or how the control signals generated by the DSP and quad converter affect the operation of the feed circuit. Therefore, Zhou anticipates all limitations of the claim with the exception of *a tip* and *a ring control circuit.*

Rosch teaches a wideband telephone line interface circuit. See Abstract. In one embodiment depicted in figure 3, DC feed circuitry is illustrated and includes both *tip control circuitry* (142) and (144) and *ring control circuitry* (148) and (150). Each of the *control circuits* is responsive to a pair of control signals that are uniquely associated with the tip and ring liens. As such, fine control is provided over the DC feed circuitry.

It would have been obvious to one of ordinary skill in the art to implement the DC feed circuitry and control using the circuitry as taught by Rosch simply because Zhou fails to disclose the necessary structure.

Claim 18 recites essentially the same subject matter as claim 7, and is rejected for the same reasons.

Claim 10 is limited to *the subscriber loop linefeed driver of claim 4*, as covered by Zhou. Again, Zhou discloses the existence of voiceband data signals that are bidirectionally coupled between the XASLIC devices and the DSP by way of the quad converter; however, Zhou does not disclose the interface. Therefore, Zhou anticipates all limitations of the claim with the exception of *voiceband circuitry.*

Rosch teaches a wideband telephone line interface circuit. See Abstract. Figure 3, in addition to the DC feed circuitry discussed in claim 7, includes an interface that provides AC signals to a respective subscriber loop by way of terminals (36). As seen clearly from figure 3, the AC interface includes a capacitor (120) and a *load* (118). The capacitor isolates the voiceband data interface from DC signals present on the subscriber loop. The interface of Rosch is *analog* as evidenced by the lack of any conversion circuitry between the loop connections 14 and the Tx and Rx ports of figure 3.

It would have been obvious to one of ordinary skill in the art to implement the voiceband circuitry of Zhou using the circuitry as taught by Rosch simply because Zhou fails to disclose the necessary structure.

Claim 11 is limited to *the subscriber loop linefeed driver of claim 10*, as covered by Zhou. Figure 3 of Rosch clearly depicts an *output node* labeled TX, a *load* (118) and a *voiceband data input node* that is *capacitively coupled* to either the tip or ring node by capacitor (136). Therefore, Zhou in view of Rosch makes obvious all limitations of the claim.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

5. **Claims 2, 6, 8, 9, 12, 17, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.**

Claim 2 is limited to *the apparatus of claim 1*, as covered by Zhou. The system of Zhou clearly indicates that the signals I_A and I_B are determined as current through line feed resistors. This implies that they are determined as a function of the voltage differential between the two resistor ends and the value of the resistor, however, the signals applied to the quad converter are single ended current values and not *differential voltages proportional to a ring current* as claimed. Thus claim 2 is allowable over Zhou.

Claim 6 recites essentially the same subject matter as claim 2, and is allowable over Zhou for at least the same reasons.

Claim 8 is limited to *the subscriber loop linefeed driver of claim 7*, as covered by Zhou. Clearly, either Zhou or Rosch does not depict the detailed structure recited by this claim. Thus, claim 8 is allowable over Zhou in view of Rosch.

Claim 9 is limited to *the subscriber loop linefeed driver of claim 8*, as covered by Zhou. Claim 9 depends on claim 8, and is allowable over Zhou in view of Rosch for at least the same reasons.

Claim 12 is limited to *the subscriber loop linefeed driver of claim 4*, as covered by Zhou. While it was shown in the rejection of claim 11 that it would have been obvious to include capacitively coupled voiceband circuitry, there is no suggestion in the prior art to modify the line card disclosed by Zhou, which transmits all data signals separately, such that audio and DC linefeed control signals are superimposed. Thus, claim 12 is allowable over Zhou in view of Rosch.

Claim 17 recites essentially the same subject matter as claim 2, and is allowable over Zhou for at least the same reasons.

Claim 19 recites essentially the same subject matter as claim 8, and is allowable over Zhou for at least the same reasons.

Claim 20 depends on claim 19, and is allowable over Zhou for at least the same reasons.

Response to Arguments

Applicant's arguments filed 18 November 2005 have been fully considered but they are not persuasive.

With respect to claims 1, 4, 13 and 15, the applicant alleges on page 9 of the current response that Zhou does not anticipate "an integrated circuit...wherein the integrated circuit generates an analog control signal," to which the examiner respectfully disagrees. In particular, while the applicant correctly notes that Zhou teaches but a single "digital" input for receiving "tip sense" and "ring sense" signals and that Zhou teaches generating a "digital control signal," the rejection made correspondence between the quad converters taught by Zhou and the "integrated circuit" of the claim, not between the DSP taught by Zhou and the "integrated circuit." As the quad converters generate an "analog control signal," Zhou anticipates all limitations of the claim. See column 7, lines 37-61.

The applicant also alleges on page 10 that the DSP of Zhou does not contain "node sets" as recited in claims 4 and 13. However, this argument is moot for the

reasons above with respect to the "analog control signal." As all of the applicant's arguments concerning these claims have been shown to be either moot or unpersuasive, the rejections of these claims are maintained.

With respect to claims 3 and 14, the applicant alleges on pages 11 and 12 of the current response that assuming *arguendo* that the functional blocks are discrete integrated circuits that interfacing with a subscriber line requires voltages in excess of traditional CMOS integrated circuit limitations, which renders the claims non-obvious, to which the examiner respectfully disagrees. As a first matter with respect to the applicant's contention that the quad converter is not an integrated circuit, Zhou discloses that the DSP comprises a "converter chip" interface 602. This directly shows that the quad converters are chips, i.e. "integrated circuits."

The applicant's remaining arguments may be applicable to the analog circuitry housed within XASLIC 504 and RC networks and protection circuit 502 of Zhou, but since quad converter 506 does not directly interface with any subscriber loop, there is no reason why the quad converter 506 should be designed to do so.

With respect to the applicant's first point of traversal: a) functional requirements of the prior art SLICs—these requirements are not directly applicable to a quad converter that doesn't provide any of the high-voltage functions of a SLIC. With respect to the applicant's second point of traversal: b) lack of any intrinsic or extrinsic evidence for the examiner's position—the AM79213/Am79C203/031 Advanced Subscriber Line Interface Circuit (ASLIC™) Device Advanced Subscriber Line Audio-Processing Circuit (ASLAC™) Device Preliminary Datasheet," Publication #19770, Rev. B, September

1998 referenced by the applicant supports the examiner's Official Notice. The first paragraph of page 13 states "a low-voltage CMOS device that combines CODEC." The quad converter of Zhou provides CODEC. As shown in the prior art, CODECs are manufactured using CMOS processes. With respect to the applicant's third point of traversal: c) extrinsic evidence from references already cited by applicant which support applicant's position—like point a), these references fail to show nonobviousness because they are not directed specifically to a quad converter. Therefore, as all of the applicant's arguments have been shown to be either moot or unpersuasive, the rejections of claims 3 and 14 are maintained.

The rejections of all claims not discussed above are maintained for the same reasons.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB

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SUPERVISORY PATENT EXAMINER